IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	Date: January 25, 2007
Andreas DOERING, et al.	Confirmation No: 8071
Serial No: 10/696,865	Group Art Unit: 2183
Filed: October 30, 2003	Examiner: Johnson, Brian P.

For: METHOD AND APPARATUS FOR USING FPGA TECHNOLOGY WITH A MICROPROCESSOR FOR RECONFIGURABLE INSTRUCTION LEVEL HARDWARE ACCELERATION

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Commissioner for Patents
P.O. Box 1450
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REQUEST FOR CONTINUED EXAMINATION UNDER 37 C.F.R. § 1.114 WITH AMENDMENT IN REPLY TO ACTION OF JULY 28, 2006

In response to the Office Action dated July 28, 2006, Applicant makes a request for continued examination under 37 C.F.R. § 1.114, and amends the application identified above as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page **2** of this paper.

Remarks begin on page **10** of this paper.